REMARKS

Reconsideration of the application is requested.

Claims 1-11 remain in the application. Claims 1-11 are subject to examination. Claims 7 and 11 have been amended.

Under the heading "Claim Objections" on page 2 of the above-identified Office Action, the Examiner objected to claim 9 because of an informality. The Examiner's suggested correction to add the word "line" has been made.

Under the heading "Claim Rejections - 35 USC § 112" on page 2 of the above-identified Office Action, claim 11 has been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner states that there is no antecedent basis for the recitation of "the first level". The terms "in the" has been changed to "at a" to overcome the antecedent issue.

It is accordingly believed that claim 11 meets the requirements of 35 U.S.C. § 112, second paragraph. The above-noted changes to the claims are provided solely for clarification or cosmetic reasons. The changes are neither

provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

Under the heading "Claim Rejections - 35 USC § 102" on pages 2-4 of the above-identified Office Action, claims 1-11 have been rejected as being fully anticipated by U.S. Patent No. 5,781,746 to Fleck (hereinafter Fleck) under 35 U.S.C. § 102.

Fleck discloses a microprocessor formed of a processing unit 2, a bus control unit 3, an internal data bus 5 and an internal control bus 6. The Examiner equates the internal buses 5 and 6 of Fleck as being the same as the lines 3 and 4 in the instant application. However, a 16 line bus and a single line are not comparable, since a bus is formed of multiple lines (compare Fleck column 1, lines 21-23 and our application, page 3, lines 9-13).

The buses described in Fleck are used to read and write byte or word-wide data, e.g. they are used for parallel communication. Our bidirectional line 4 is used for serial communication, instead (another indication that line 4 is just a single line).

Regarding claims 1 and 6 of the instant application, it is

recited that the second line is placeable in a dominant state by the logic circuit when a data transmission is to be made by the logic circuit. Simply put, this mode or feature is not believed to be taught in Fleck as this mode applies to serial communications. The Examiner is respectfully requested to identify the column and line in Fleck discussing this matter.

Furthermore, the steps according to claims 1 to 5 of the instant application are not believed to be described by Fleck because they do not apply to a parallel communication system.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 and 6. Claims 1 and 6 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 6.

In view of the foregoing, reconsideration and allowance of claims 1-11 are solicited.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith

should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

For Applicants

REL:cgm

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